IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No. 040301/0487

In re reissue patent application of

Nobuo FUDANUKI et al.

Serial No: Not Yet Assigned

Application for reissue of U.S. Patent No. 6,054,872, granted April 25, 2002

Filed: Herewith

For: SEMICONDUCTOR INTEGRATED CIRCUIT WITH MIXED GATE ARRAY AND STANDARD CELL

ASSENT OF ASSIGNEE

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned assignee of the entire right, title and interest to the United States Letters Patent 6,054,872 hereby assents to the accompanying reissue application and offer to surrender said Letters Patent.

Date: September 7, 2001

Name: Takashi Nakayama

Title: General Manager, Intellectual Property Division

Signature: _____

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BROADENING REISSUE DECLARATION UNDER 37 C.F.R. §1.175

Commissioner for Patents
Washington, D.C. 20231

Sir:

We, Nobuo Fudanuki and Toshikazu Sei, declare that:

1. Our residence, post office address and citizenship are stated below next to our names.

2. We believe we are the original and first inventors and sole inventors of the subject matter described and claimed in my U.S. Patent 6,054,872 and in the foregoing specification for which a reissue patent is sought on the invention entitled SEMICONDUCTOR INTEGRATED CIRCUIT WITH MIXED GATE ARRAY AND STANDARD CELL.

3. We have reviewed and understand the contents of the above-identified

specification, including the claims.

4. We acknowledge the duty to disclose information which is material to examination of the application in accordance with 37 C.F.R. §1.56(a).

5. We believe U.S. Patent No. 6,054,872 ("the '872 patent") is wholly or partly inoperative or invalid by reason of our claiming less than we had the right to claim in the patent.

6. One specific error was for us not to include claims which recite:

(Reissue Claim 22) The integrated circuit of claim 1, wherein each gate array basic cell has the same pattern of gate electrodes and the same pattern of impurity regions.

(Reissue Claim 23) The integrated circuit of claim 1, wherein said standard cells include a third type cell having a width different from the widths of the first type cell and the second type cell.

(Reissue Claim 24) The integrated circuit of claim 19, wherein each gate array basic cell has the same pattern of gate electrodes and the same pattern of impurity regions.

(Reissue Claim 25) The integrated circuit of claim 19, wherein said standard cells include a third type cell having a width different from the widths of the first type cell and the second type cell.

(Reissue Claim 26) The integrated circuit of claim 19, wherein the basic cells are used to construct additional circuits for increasing driving capability to drive signals transmitted to a plurality of circuits disposed on a semiconductor substrate.

(Reissue Claim 27) The integrated circuit of claim 19, wherein respective cell rows are arranged adjacently.

(Reissue Claim 28) The integrated circuit of claim 19, wherein the standard cells and the basic cells have common power supply lines arranged along a straight line.

(Reissue Claim 29) The integrated circuit of claim 19, wherein widths of the standard cells are integral multiple of a width of the basic cells.

(Reissue Claim 30) A semiconductor integrated circuit comprising:

a plurality of standard cells arranged in each of a plurality of adjacent cell rows, said plurality of standard cells in each row having at least two different widths; and

a plurality of gate array basic cells arranged in said cell rows in which said standard cells are arranged, each gate array basic cell having the same pattern of gate electrodes and the same pattern of impurity regions so that a width of each gate array basic cell is equal to each other,

wherein said width of each gate array basic cell is substantially identical to a first one of the at least two different widths of said standard cells.

(Reissue Claim 31) The integrated circuit of claim 30, wherein the plurality of standard cells have at least three different widths.

(Reissue Claim 32) The integrated circuit of claim 30, wherein a second one of the at least two different widths of said standard cells is substantially identical to an integral multiple of said width of said gate array basic cell.

(Reissue Claim 33) The integrated circuit of claim 30, wherein in each row, a first impurity diffusion region and a second impurity diffusion region are arranged in the direction of said cell rows, said standard cells and gate array basic cells being arranged in said first and second impurity diffusion regions.

(Reissue Claim 34) The integrated circuit of claim 33, wherein said first and second impurity diffusion regions are well regions.

(Reissue Claim 35) The integrated circuit of claim 33, wherein each cell row has a first row and a second row adjacent to each other, in each cell row the first impurity diffusion region is arranged in one of the first and second rows and the second impurity diffusion region is arranged in the other of the first and second rows.

(Reissue Claim 36) The integrated circuit of claim 35, wherein at least one cell row has the first impurity diffusion region in the first row, and at least one cell row has the first impurity diffusion region in the second row.

(Reissue Claim 37) The integrated circuit of claim 35, further comprising power supply wirings for supplying power to said standard cells and gate array basic cells, disposed above said adjacency of said first and second rows.

(Reissue Claim 38) The integrated circuit of claim 37, wherein said power supply wirings are made of a first-metal wiring layer.

(Reissue Claim 39) The integrated circuit of claim 38, wherein said standard cells and said gate array basic cells are wired by wirings made of at least said first-metal wiring layer, second and third-metal wiring layers disposed above said first-metal wiring layer in order.

(Reissue Claim 40) The integrated circuit of claim 39, wherein a width of said power supply wirings is at least twice as wide as a width of said wirings.

(Reissue Claim 41) The integrated circuit of claim 38, wherein said wirings made of said first and second-metal wiring layer are disposed in direction parallel to said cell rows, and said wirings made of said third-metal wiring layer are disposed in direction perpendicular to said cell rows.

(Reissue Claim 42) The integrated circuit of claim 33, wherein each of said first and second impurity diffusion regions has a contact region of the same impurity type therein, wherein an impurity concentration of said contact region is higher than in of each of the first and second impurity diffusion regions.

(Reissue Claim 43) The integrated circuit of claim 30, wherein the gate array basic cells are used to construct intermediate buffers for distributing a clock signal to a plurality of circuits which are displaced on a semiconductor substrate.

(Reissue Claim 44) The integrated circuit of claim 30, wherein the gate array cells are used to construct additional circuits for increasing driving capability to drive signals transmitted to a plurality of circuits disposed on a semiconductor substrate.

(Reissue Claim 45) The integrated circuit of claim 30, further comprising at least one of megacell and megafunction in another area of a plurality of cell rows on a single semiconductor chip .

(Reissue Claim 46) The integrated circuit of claim 45, wherein said megacell is one of ROM or RAM or both, and said megafunction is one of ALU or CPU or both.

(Reissue Claim 47) A semiconductor integrated circuit having a logic circuit area and at least one of megacell and megafunction on a single semiconductor chip, the logic circuit area comprising:

a plurality of standard cells arranged in each of a plurality of adjacent cell rows, said plurality of standard cells in each row having at least two different widths; and

a plurality of gate array basic cells arranged in said cell rows in which said standard cells are arranged, each gate array basic cell having the same pattern of gate electrode and the same pattern of impunity regions,

wherein said width of each gate array basic cell is substantially identical to a first one of the at least two different widths of said standard cells.

(Reissue Claim 48) The integrated circuit of claim 47, wherein a second one of the at least two different widths of said standard cells is substantially identical to an integral multiple of said width of said gate array basic cell.

(Reissue Claim 49) The integrated circuit of claim 48, wherein a height of said standard cells is substantially identical to a height of said gate array basic cells.

(Reissue Claim 50) The integrated circuit of claim 47, wherein each row, a first impurity diffusion region and a second impurity diffusion region are arranged in the direction of said cell rows, said standard cells and gate array basic cells being arranged in said first and second impurity diffusion regions.

(Reissue Claim 51) The integrated circuit of claim 50, wherein said first and second impurity diffusion regions are well regions.

(Reissue Claim 52) The integrated circuit of claim 50, wherein each cell row has a first row and a second row adjacent to each other, in each cell row the first

impurity diffusion region is arranged in one of the first and second rows and the second impurity diffusion region is arranged in the other of the first and second rows.

(Reissue Claim 53) The integrated circuit according to claim 52, wherein at least one cell row has the first impurity diffusion regions in the first row, and at least one cell row has first the impurity diffusion region in the second row.

(Reissue Claim 54) The integrated circuit of claim 50, further comprising power supply wirings for supplying power to said standard cells and gate array basic cells, disposed above said adjacency of said first and second rows.

(Reissue Claim 55) The integrated circuit of claim 54, wherein said power supply wirings are made of first-metal wiring layer.

(Reissue Claim 56) The integrated circuit of claim 55, wherein said standard cells and said gate array basic cells are wired by wirings made of at least said first-metal wiring layer, second and third-metal wiring layer disposed above said first-metal wiring layer in order.

(Reissue Claim 57) The integrated circuit of claim 56, wherein a width of said power supply wirings is at least twice as wide as a width of said wirings.

(Reissue Claim 58) The integrated circuit of claim 56, wherein said wirings made of said first and second-metal wiring layer are disposed in direction parallel to said cell rows, and said wirings made of said third-metal wiring layer are disposed in direction perpendicular to said cell rows.

(Reissue Claim 59) The integrated circuit of claim 50, wherein each said first and second diffusion regions has contact region of the same impurity type therein,

wherein an impurity concentration of said contact region is higher than it of each diffusion regions.

(Reissue Claim 60) The integrated circuit of claim 47, wherein the gate array basic cells are used to construct intermediate buffers for distributing a clock signal to a plurality of circuits which are displaced on a semiconductor substrate.

(Reissue Claim 61) The integrated circuit of claim 47, wherein the gate array basic cells are used to construct additional circuits for increasing driving capability to drive signals transmitted to a plurality of circuits disposed on a semiconductor substrate.

(Reissue Claim 62) The integrated circuit of claim 47, wherein said megacell is one of ROM or RAM or both, and said megafunction is one of ALU or CPU or both.

(Reissue Claim 63) The integrated circuit of claim 47, wherein said standard cells and said gate array basic cells are arranged over substantial entire region of each said cell rows, edges of each said cell rows are in straight line.

(Reissue Claim 64) The integrated circuit of claim 63, wherein said at least one of megacell and megafunction has a rectangular pattern, edges of each said cell rows of and one side of said rectangular pattern are in straight line.

(Reissue Claim 65) The integrated circuit of claim 47, wherein the plurality of standard cells have at least three different widths.

7. By this reissue declaration, we desire to seek broadened claims, and, this application for reissue of the original Letters Patent addresses the aforementioned error by including new independent claims 30 and 47, which do not recite an unnecessary feature of specifying the height and shape of the gate array basic cells and the standard

cells, and by adding new dependent claims 22-29, 31-46 and 47-64 to define the system of the present invention with the variety in scope and the degree of specificity necessary to adequately protect the invention. Support for the new claims 22-64 exists in Figures 3A-3D, 5A-5B and 11 of the Letters Patent and in column 7, lines 37-49 and column 8, line 19 - column 9, line 49 of the specification.

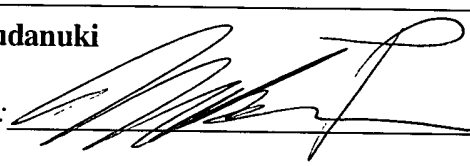
8. All errors that are being corrected up to the time of the filing of the Declaration in this reissue application arose without any deceptive intention on our part.

WHEREFORE, we pray that we may be allowed to surrender the original Letters Patent 6,054,872 and do hereby offer same.

We hereby appoint Stephen A. Bent, Reg. No. 29,768; David A. Blumenthal, Reg. No. 26,257; William T. Ellis, Reg. No. 26,874; John J. Feldhaus, Reg. No. 28,822; Peter G. Mack, Reg. No. 26,001; Brian J. McNamara, Reg. No. 32,789; Sybil Meloy, Reg. No. 22,749; George E. Quillin, Reg. No. 32,792; Bernhard D. Saxe, Reg. No. 28,665; Charles F. Schill, Reg. No. 27,590; Richard L. Schwaab, Reg. No. 25,479; Harold C. Wegner, Reg. No. 25,258, Glenn Law, Reg. No. 34,371, Beth A. Burrous, Reg. No. 35,087, Lyle K. Kimms, Reg. No. 34,079, Johnny A. Kumar, Reg. No. 34,649, and Marc K. Weinstein, Reg. No. 43,250 as my attorneys with full power of substitution and revocation to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected herewith, and request that all correspondence be sent to FOLEY & LARDNER, 3000 K Street, N.W., Suite 500, Washington, DC 20007-5109 at (202) 672-5300.

The undersigned petitioner declares further that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Nobuo Fudanuki

Signature:  *Date:* Aug 31, 2001

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Toshikazu Sei

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